Hi3719M V100 Brief Data Sheet

Key Specifications

Processor Architecture

- Dual-CPU
  - ARM Cortex A9 CPU
  - Dedicated HiFi audio processor, supporting high-performance audio processing of Dolby7.1 and DTS Master Audio
- Dual-GPU architecture, supporting 1080p full-HD GUI and games

CPU

- ARM Cortex A9 processor
- Independent I-cache, D-cache, and L2 cache
- Integrated multimedia acceleration engine NEON
- Hardware Java acceleration
- Integrated hardware floating-point coprocessor

3D GPU

- Dual-core high-performance GPU
- OpenGL ES 2.0/1.1/1.0 and OpenVG 1.1
- EGL

Memory Interfaces

- DDR3/3L SDRAM interface
  - Maximum 1 GB memory capacity
  - 16-bit or 32-bit memory width
  - Maximum 800 MHz or 1600 MHz frequency
- SPI flash interface
  - 1-/2-/4-bit flash memory
  - Maximum 32 MB SPI flash capacity
- NAND flash interface
  - SLC/MLC flash memory
  - Toggle 1.0/2.0 or ONFI 2.0/3.0
  - 8-bit data width
  - Maximum 64 GB NAND flash capacity
  - Maximum 80-bit ECC
- eMMC flash interface

Video Decoding

- H.264 BP/MP/HP@ level 5.0; MVC
- MPEG1
- MPEG2 SP@ML and MP@HL
- MPEG4 SP@L0–3 and ASP@L0–5; GMC
- MPEG4 short header format (H.263 baseline)
- AVS baseline @level 6.0 and AVS+ (AVS-P16)
- VC-1 SP@ML, MP@HL, and AP@L0-3
- VP6/VP8
- 1080p@60 fps decoding
- Low-delay decoding
- Simultaneous multi-channel decoding

Image Decoding

- Full HD JPEG hardware decoding, a maximum of 64 megapixels
- MJPEG baseline decoding
- PNG hardware decoding, a maximum of 64 megapixels

Video and Image Encoding

- H.264 BP/MP/HP@level 4.2 video encoding, a maximum of 720p@30 fps encoding capability
- JPEG hardware encoding, a maximum of 720p@30 fps encoding capability
- VBR or CBR mode for video decoding
- Inter-frame prediction and intra-frame prediction
- Fast motion estimation algorithm
- Low-delay encoding
- Encoding of multiple ROIs

Audio Encoding and Decoding

- Dedicated audio DSP
- G.711(u/a) audio decoding
- MPEG L1/L2
- DRA decoding
- Dolby Digital and Dolby Digital Plus
- Dolby True HD and Dolby Digital Plus transcoding
- DTS and DTS HD core decoding
- DTS and Dolby Digital transparent transmission
- AAC-LC and HE AAC V1/V2 decoding
- APE, FLAC, Ogg, AMR-NB, and AMR-WB decoding
- Down mixing and resampling
- 2-channel audio mixing and echo cancellation
- Intelligent volume control
- SRS, Dolby, and MS11 sound effects
- Pounding bass processing
- G.711(u/a), AMR-NB, AMR-WB, and AAC-LC encoding

TS Demultiplexing/PVR

- Two TS inputs
- A maximum of 96 hardware PID channels

Security Processing

- Advanced security features
- DRM
- OTP
- AES, DES, and 3DES data encryption and decryption
- Hardware hash algorithm
- Content protection for USB devices

Graphics and Display Processing

- Hardware overlaying of multi-channel graphics and video inputs
- 5-layer OSD
- Four video layers
- Mosaic and multi-region display
- Mirroring display
- 16-bit or 32-bit color depth
- Video rotation
- Letterbox and pan and scan
- 3D video processing and display
- Multi-tap vertical and horizontal scaling of videos and graphics; free scaling
- Low-delay display

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- Enhanced full-hardware TDE
- Full-hardware anti-aliasing and anti-flicker
- CSC with configurable coefficients
- Image enhancement and denoising
- Deinterlacing
- Sharpening
- Chrominance, luminance, contrast, and saturation adjustment
- Video Db/Dr processing

Audio and Video Interfaces

- PAL, NTSC, and SECAM standard output, and forcible standard conversion
- Aspect ratio of 4:3 or 16:9 and forcible aspect ratio conversion
- 1080p60/1080p50/1080p30/1080p24/1080i60/1080i50 /720p/576p/576i/480p/480i outputs
- One SD output and one HD output from the same source or different sources
- Digital video interfaces
- One HDMI 1.4a TX with HDCP1.2 output interface
- Analog video interfaces
  - One CVBS interface
  - One YPbPr or VGA interface
  - Four embedded VDACs that support cable detection
  - Configurable CVBS or YPbPr output for each VDAC
  - Rovi and VBI
- Audio interfaces
  - Audio-left and audio-right channels
  - SPDIF interface
  - Embedded ADAC
  - One I^2S or PCM digital audio input/output
  - HDMI audio output

Peripheral Interfaces

- Two USB 2.0 host ports, one supporting the host/device function
- One 4-bit SDIO 3.0 interface with integrated LDO, supporting 3.3 V or 1.8 V components
- One 10/100 Mbit/s MAC with an integrated Fast Ethernet PHY
- One IR receiver with two input interfaces
- One LED and keypad control interface
- Three I^2C interfaces
- Multiple UART interfaces
- Multiple GPIO interfaces
- One PWM interface
- Integrated POR module

Others

- 2-layer PCB design
- Various boot modes
- Boot program download and execution over a serial port or USB port
- Integrated standby processor, supporting various low-power modes and less than 30 mW standby power consumption
- Low-power design such as AVS and DVFS
- BGA 19 mmx19 mm package

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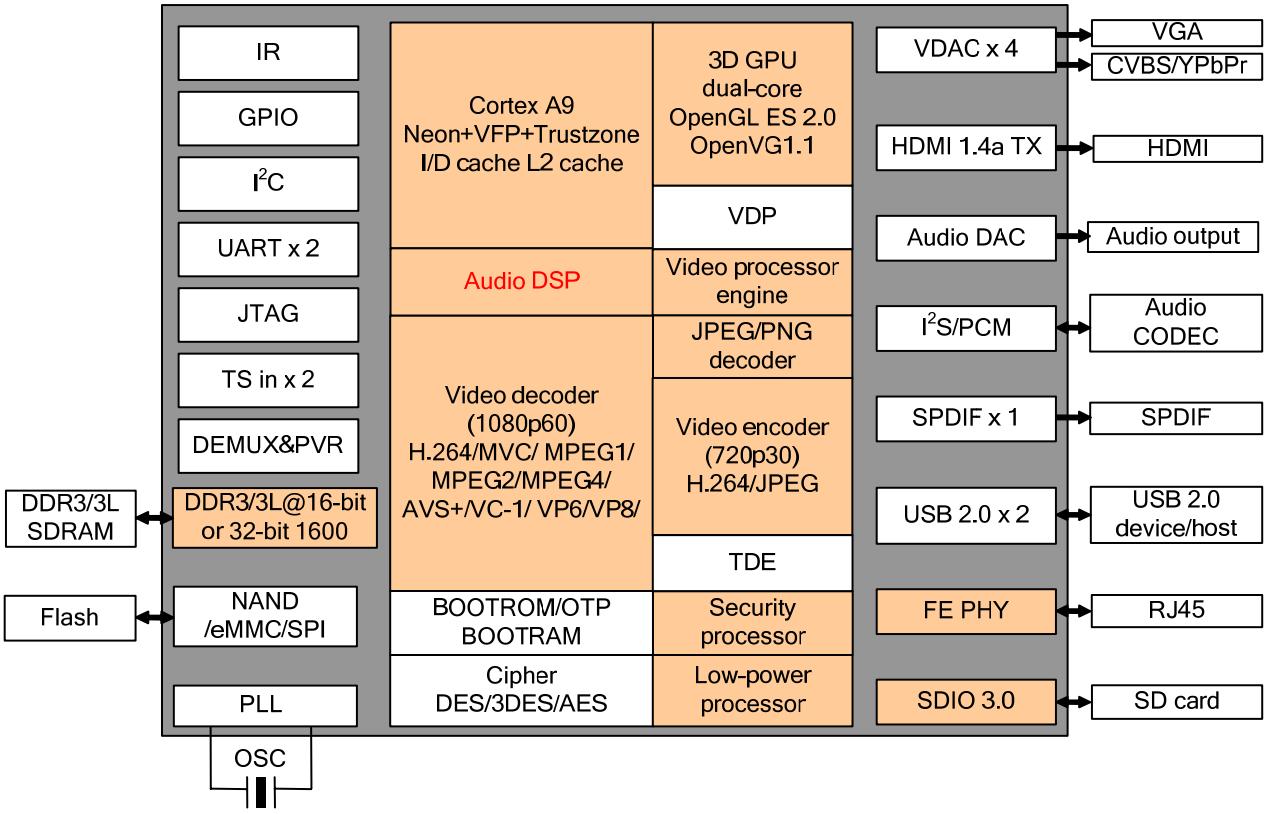
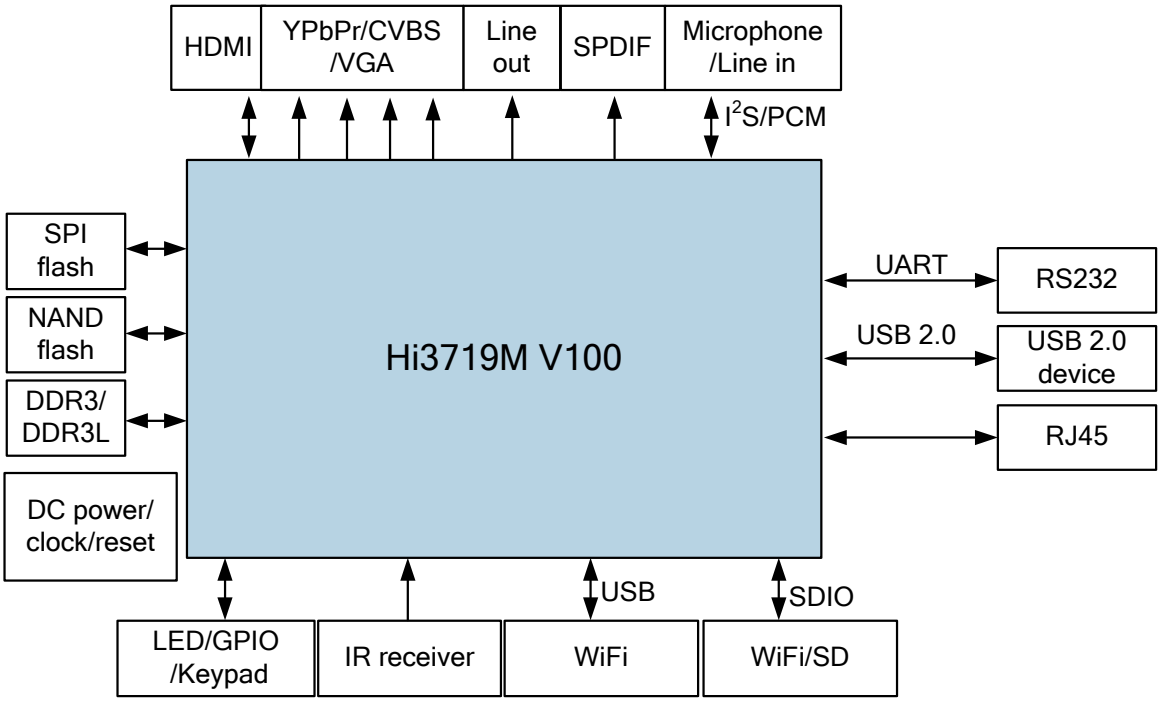
Functional Block Diagram



With an integrated high-performance Cortex A9 processor and embedded NEON, Hi3719M V100 meets differentiated service requirements. Dedicated HiFi audio processor, supporting high-performance audio processing of Dolby7.1 and DTS Master Audio. To meet the growing requirements on multimedia playback, video communication, and multi-screen transcoding, Hi3719M V100 supports HD video decoding in various formats, including H.264, MVC, MPEG1, MPEG2, MPEG4, AVS+, VC-1, VP6, and VP8, and high-performance H.264 HD encoding. Hi3719M V100 provides a smooth man-machine interface and rich gaming experience with a high-performance 2D/3D acceleration engine. It also enables flexible connection schemes with one Ethernet port, two USB ports, and more peripheral interfaces.

Typical Application Block Diagram



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Acronyms and Abbreviations

ADAC	audio DAC
AES	advanced encryption standard
AVS	audio/video coding standard
AVS	adaptive voltage scaling
CABAC	context-based adaptive binary arithmetic coding
CBR	constant bit rate
CSC	color space conversion
CVBS	composite video broadcast signal
DES	data encryption standard
DRM	digital rights management
DSP	digital signal processor
DVFS	dynamic voltage and frequency scaling
GPIO	general purpose input/output
GPU	graphics processing unit
HDCP	high-bandwidth digital content protection
HDMI	high definition multimedia interface
I/O	input/output
I^2C	inter-integrated circuit
I^2S	inter-IC sound
IR	infrared
LCD	liquid crystal display
MLC	multi-level cell
OTP	one-time programmable
PBGA	plastic ball grid array
PCM	pulse code modulation
PID	packet ID
POR	power-on reset
PVR	personal video recorder
PWM	pulse width modulation
ROI	region of interest
SLC	single-level cell
SPDIF	Sony/Philips digital interface
UART	universal asynchronous receiver transmitter
VBR	variable bit rate
VDAC	video digital-to-analog converter